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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/428,052	10/27/1999	KIYOSHI IRINO	970901A	4139

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EXAMINER

DIAZ, JOSE R

ART UNIT	PAPER NUMBER
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2815

DATE MAILED: 03/01/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/428,052

Applicant(s)

IRINO, KIYOSHI

Examiner

José R. Díaz

Art Unit

2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 January 2002.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 6, 10-13, 15 and 16 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 15 and 16 is/are allowed.
- 6) ☒ Claim(s) 6 and 10-13 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☒ Certified copies of the priority documents have been received in Application No. 08/917,936.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Continued Prosecution Application

➤ The request filed on January 9, 2002 for a Continued Prosecution Application (CPA) under 37 CFR 1.53(d) based on parent Application No. 09/428,052 is acceptable and a CPA has been established. An action on the CPA follows.

Claim Objections

➤ Claim 13 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. The limitations disclosed in claim 13 are included in the new amended claim 6.

Claim Rejections - 35 USC § 102

➤ The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily

published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

➤ Claims 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Hause et al. (US Patent No. 5,861,335).

Regarding claim 10, Hause et al. teach a method of manufacturing a semiconductor device comprising the steps of: forming a gate oxide film (20a) on a substrate (12) (see Fig. 1); forming a gate electrode pattern (18a) (see Fig. 1); forming diffusion regions (26) (see Fig. 3 and col. 6, lines 19-40); and implanting N ions and annealing said gate oxide (see col. 6, lines 35-67).

Claim Rejections - 35 USC § 103

➤ The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

➤ Claims 6 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hause et al. (US Patent No. 5,861,335) in view of Bhat et al. ("Performance and Hot-Carrier Reliability of N- and P- MOSFETs with Rapid Thermally NO-nitrided SiO₂ Gate Dielectrics", IEEE, 1994, pp. 12.3.1-12.3.3).

Regarding claims 6 and 13, Hause et al. teach a method of manufacturing a semiconductor device comprising the steps of: forming a gate oxide film (20a) on a substrate (12) (see Fig. 1); forming a gate electrode pattern (18a) (see Fig. 1); forming

Art Unit: 2815

diffusion regions (26) (see Fig. 3 and col. 6, lines 19-40); and annealing said gate oxide in an nitrogen ambient at about 800 °C (see col. 6, lines 35-67, col. 7, lines 33-38, and col. 9, lines 10-15). However, Hause et al. fail to teach the limitation of annealing in an atmosphere containing NO. Bhat et al. teach that is well known in the art to introduce nitrogen in a gate oxide film by annealing in a NO ambient (see publication "Performance and Hot-Carrier Reliability of N- and P- MOSFETs with Rapid Thermally NO-nitrided SiO₂ Gate Dielectrics", pp. 12.3.1-12.3.3). Therefore, it would have been obvious to one having ordinary skill in the art at the same time the invention was made to modify Hause et al. to include the step of annealing the gate oxide in an atmosphere containing NO. The ordinary artisan would have been motivated to modify Hause et al. in the manner described above for at least the purpose of incorporating nitrogen (N) in the gate oxide film without a significant increase in oxide thickness.

➤ Claims 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hause et al. (US Patent No. 5,861,335) in view of Arai et al. (US Patent No. 5,972,783)

Regarding claims 11 and 12, Hause et al. fails to teach an acceleration voltage and an implant dose of the ion implantation process. Arai et al. teach that is well known in the art to implant nitrogen in a gate oxide by implanting under the following parameters: an acceleration voltage of at least 5KeV and an implant dose of at least $1 \times 10^{13} \text{ cm}^{-2}$ (see col.12, lines 45-64). Therefore, it would have been obvious to one having ordinary skill in the art at the same time the invention was made to modify Hause et al. to include the step of implanting nitrogen at an acceleration voltage of at least 5KeV and an implant dose of at least $1 \times 10^{13} \text{ cm}^{-2}$. The ordinary artisan would have been

Art Unit: 2815

motivated to modify Hause et al. in the manner described above for at least the purpose of incorporating nitrogen ions into both edges of the gate oxide film.

➤ Claims 6 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tseng et al. (US Patent No. 5,726,087) in view of Bhat et al. ("Performance and Hot-Carrier Reliability of N- and P- MOSFETs with Rapid Thermally NO-nitrided SiO₂ Gate Dielectrics", IEEE, 1994, pp. 12.3.1-12.3.3).

Regarding claims 6 and 13, Tseng et al. teach a method of manufacturing a semiconductor device comprising the steps of: forming a gate oxide film (14, 16) on a substrate (12) (see Fig. 12); forming a gate electrode pattern (20) (see Fig. 12); forming diffusion regions (22) (see Fig. 12); and annealing said gate oxide in an nitrogen ambient (see col. 5, lines 21-40). However, Tseng et al. fail to teach the limitation of annealing in an atmosphere containing NO at about 800 °C. Bhat et al. teach that is well known in the art to introduce nitrogen in a gate oxide film by annealing in a NO ambient at 1000 °C (see publication "Performance and Hot-Carrier Reliability of N- and P- MOSFETs with Rapid Thermally NO-nitrided SiO₂ Gate Dielectrics", pp. 12.3.1-12.3.3). Therefore, it would have been obvious to one having ordinary skill in the art at the same time the invention was made to modify Tseng et al. to include the step of annealing the gate oxide in an atmosphere containing NO at about 1000 °C. The ordinary artisan would have been motivated to modify Tseng et al. in the manner described above for at least the purpose of incorporating nitrogen (N) in the gate oxide film without a significant increase in oxide thickness. Furthermore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to perform such an

Art Unit: 2815

annealing process at a lower temperature such as 800 °C, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

➤ Claims 10-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tseng et al. (US Patent No. 5,726,087) in view of Arai et al. (US Patent No. 5,972,783).

Regarding claims 10-13, Tseng et al. teach a method of manufacturing a semiconductor device comprising the steps of: forming a gate oxide film (14, 16) on a substrate (12) (see Fig. 12); forming a gate electrode pattern (20) (see Fig. 12); forming diffusion regions (22) (see Fig. 12); and heating said gate oxide in an nitrogen ambient to introduce N atoms into said gate oxide (see col. 5, lines 21-40). However, Tseng et al. fail to teach the limitation of introducing N atoms into the gate oxide by the steps of implanting N ions and annealing the gate oxide. Arai et al. teach that is well known in the art to implant nitrogen in a gate oxide by implanting under the following parameters: an acceleration voltage of at least 5KeV and an implant dose of at least $1 \times 10^{13} \text{ cm}^{-2}$ and then, diffusing the N ions by an annealing treatment (see col.12, lines 45-64). Therefore, it would have been obvious to one having ordinary skill in the art at the same time the invention was made to modify Tseng et al. to include the step of implanting nitrogen at an acceleration voltage of at least 5KeV and an implant dose of at least $1 \times 10^{13} \text{ cm}^{-2}$. The ordinary artisan would have been motivated to modify Tseng et al. in the manner described above for at least the purpose of incorporating nitrogen ions into the gate oxide film to improve hot carrier immunity.

Allowable Subject Matter

- Claims 15-16 are allowed.

Response to Arguments

- Applicant's arguments with respect to claims 6 and 10-13 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

- The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Hwang (US Pat. No. 5,512,519) discloses method of forming a silicon-insulating layer in a semiconductor device by a NO process. Takahashi Hiroshi (JP 10-189949) disclose annealing a gate oxide in a NO ambient.

Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R. Díaz whose telephone number is (703) 308-6078. The examiner can normally be reached on 9:00 - 5:00 Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 746-3891 for After Final communications.

Application/Control Number: 09/428,052
Art Unit: 2815

Page 8

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JRD
February 25, 2002

A handwritten signature in black ink, appearing to read 'Eddie Lee', is positioned above the printed name and title.

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800